

Introduction

The sample-and-hold or track-and-hold function is very widely used in linear systems. This function is readily available in modular, hybrid, and monolithic form.

All high quality sample-and-hold circuits must meet certain requirements:

1. The holding capacitor must charge up and settle to its final value as quickly as possible.
2. When holding, the leakage current at the capacitor must be as near zero as possible to minimize voltage drift with time.
3. Other sources of error must be minimized.

Design of a sample-and-hold involves a number of compromises in the above requirements. The amplifier or other device feeding the analog switch must have high current capability and be able to drive capacitive loads with stability. The analog switch must have both low ON resistance and extremely low OFF leakage currents. But, leakage currents of most analog switches (except the dielectrically isolated types) run to several hundred nanoamperes at elevated temperatures. The analog switch must have very low coupling between the digital input and analog output, because any spikes generated at the instant of turn-off will change the charge on the capacitor. The output amplifier must have extremely low bias current over the temperature range, and also must have low offset drift and sufficient slew rate.

Another design consideration is whether to make the input differential or single ended. A single ended sample/hold amplifier has a fixed gain, usually +1, so that it simply provides the sample/hold function. In contrast, a differential input sample-and-hold amplifier is designed to be configured with external feedback, just like an op amp. It may be used to form a filter, integrator, inverting or non-inverting amplifier with gain, etc. This allows the designer to combine any number of op amp signal conditioning circuits with the sample-and-hold function. All Intersil sample-and-hold amplifiers are designed with differential inputs to take advantage of this capability.

The HA-2420/2425

The HA-2420/2425 is one of the most versatile monolithic sample-and-hold integrated circuits. A functional diagram is shown in Figure 1.

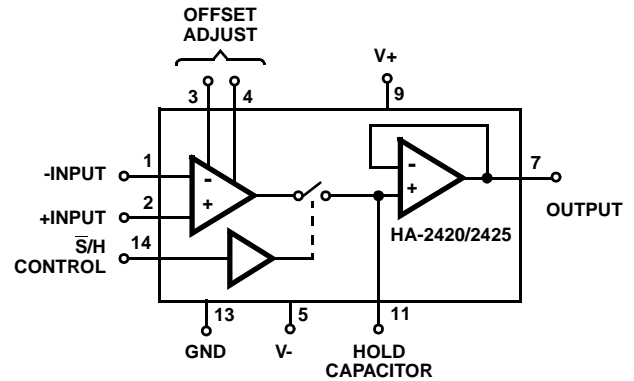


FIGURE 1. HA-2420/2425 FUNCTIONAL DIAGRAM

The input amplifier stage is a high performance operational amplifier with excellent slew rate, and the ability to drive high capacitance loads without instability. The switching element is a highly efficient bipolar transistor stage with extremely low leakage in the OFF condition. The output amplifier is a MOSFET input unity gain follower to achieve extremely low bias current.

MOSFET inputs are generally not used for DC amplifiers because their offset voltage drift is difficult to control. In this configuration, however, negative feedback is generally applied between the output and inputs of the entire device, and the effect of this offset drift at the inputs is divided by the open loop gain of the input amplifier stage.

The HA-5320

The HA-5320 is a high speed monolithic sample/hold circuit which includes its own 100pF hold capacitor. Unlike the HA-2420/2425, this device utilizes an input transconductance amplifier and integrating output stage as shown in Figure 2. The hold capacitor is charged through a low leakage analog switch at the virtual ground node of the output amplifier. In this configuration, charge injection at the transition from sample to hold is constant over the entire input/output voltage range. Additional hold capacitance may be added to the HA-5320 for improved droop rate, at the expense of increased acquisition time.

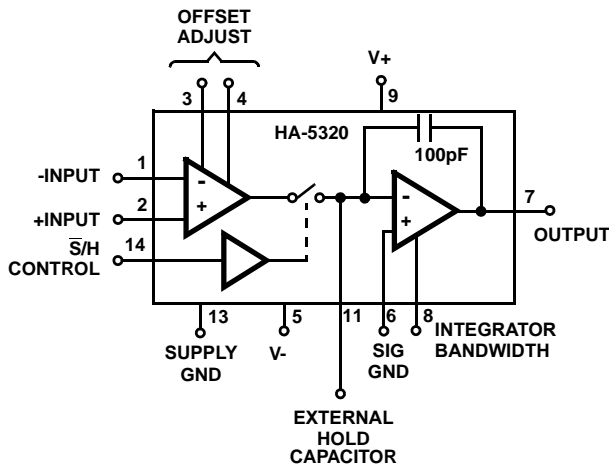


FIGURE 2. HA-5320 FUNCTIONAL DIAGRAM

The HA-5330

The HA-5330 is a monolithic sample/hold amplifier optimized for very high speed performance, acquiring a 10V step to 0.01% in 500ns. Its circuit topology is similar to the HA-5320 (Figure 3), but there is no provision for external capacitance. The integrated 90pF capacitor provides excellent performance alone; external leakage paths and noise pickup are avoided in this design by not exposing the integrator input node to an external pin.

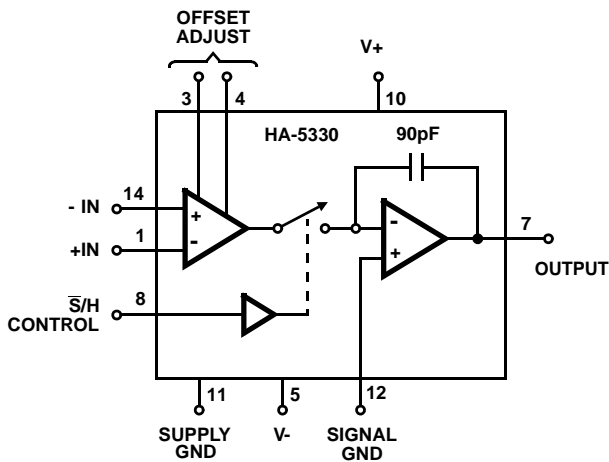


FIGURE 3. HA-5330 FUNCTIONAL DIAGRAM

Sample-and-Hold Applications

A number of basic applications are shown on the following pages. These devices are exceptionally versatile, since they can be wired into any of the hundreds of feedback configurations possible with any operational amplifier. In many applications the device will replace both an operational amplifier and a sample-and-hold module.

The larger the value of the hold capacitor, the longer time it will hold the signal without excessive drift; however, it will also reduce the charging rate/slew rate and the amplifier

bandwidth during sampling. So, the capacitance value must be optimized for each particular application. Drift during holding tends to double for every 10°C rise in ambient temperature. The holding capacitor should have extremely high insulation resistance and low dielectric absorption—polystyrene (below +85°C), Teflon, or mica types are recommended.

For least drift during holding, leakage paths on the P.C. board and on the device package surface must be minimized. The output voltage is nearly equal to the voltage on C_H for the HA-2420. The output line may be used as a guard ring surrounding the line to C_H . Since the potentials are nearly equal, very low leakage currents will flow. The two package pins surrounding the C_H pin are not internally connected, and may be used as guard pins to reduce leakage on the package surface. A suggested P.C. guard ring layout is shown in Figure 4. The hold capacitor in the HA-5320 operates at virtual ground. For this device, a guard ring must be connected to the SIG GND terminal (pin 6) instead of output.

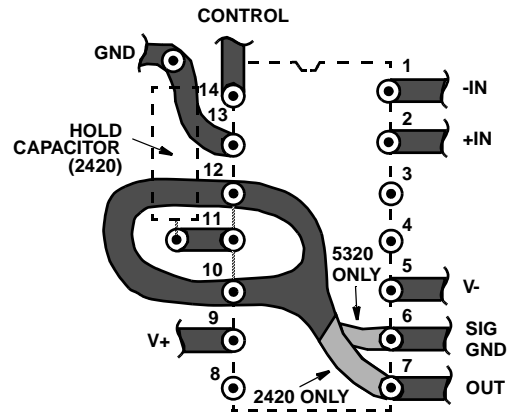


FIGURE 4. GUARD RING LAYOUT (BOTTOM VIEW)

Since the internal hold capacitor is not assessable in the HA-5330, no P.C. layout consideration to minimize leakage is necessary.

Although the hold capacitor is configured differently for the three sample/hold devices as shown in Figure 5, most applications are common to all. For simplicity, the hold capacitor has been excluded from circuit diagrams in the following examples and the S/H's are depicted as op amps with a sample/hold control. This symbol is intended to remind the user of the "op amp" capability of these devices.

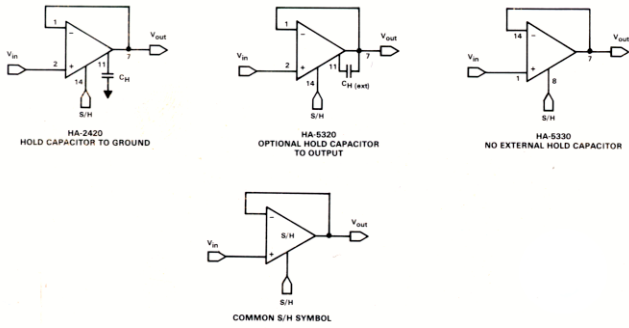


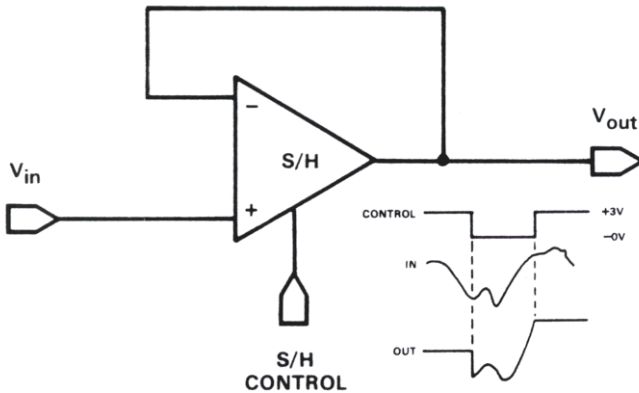
FIGURE 5. SIMPLIFIED S/H SYMBOL (UNITY GAIN CONFIGURATION)

Application No. 1

Feedback is the same as a conventional op amp voltage follower which yields a unity gain, non-inverting output. This hookup also has a very high input impedance.

The only difference between a track-and-hold and sample-and-hold is the time period during which the switch is closed. In track-and-hold operation, the switch is closed for a relatively long period during which the output signal may change appreciably; the output will hold the level present at the instant the switch is opened. In sample-and-hold operation, the switch is closed only for the period of time necessary to fully charge the holding capacitor.

BASIC TRACK-AND-HOLD/SAMPLE-AND-HOLD



Application No. 2

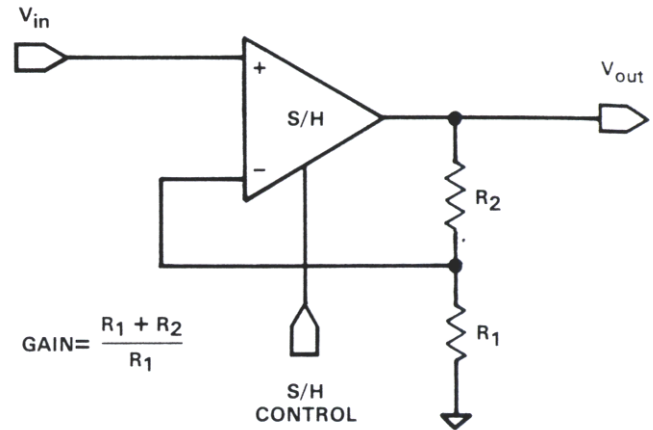
This is the standard non-inverting amplifier feedback circuit.

It illustrates one of the many ways in which a sample/hold amplifier may be used to perform both op amp and sampling functions, eliminating the need for a separate scaling amplifier and sample-and-hold module.

In general, it is usually best design practice to scale the gain such that the largest expected signal will give an output close to + or -10 volts. Drift current is essentially

independent of output level, and less percentage drift will occur in a given time for a larger output signal.

SAMPLE-AND-HOLD WITH GAIN

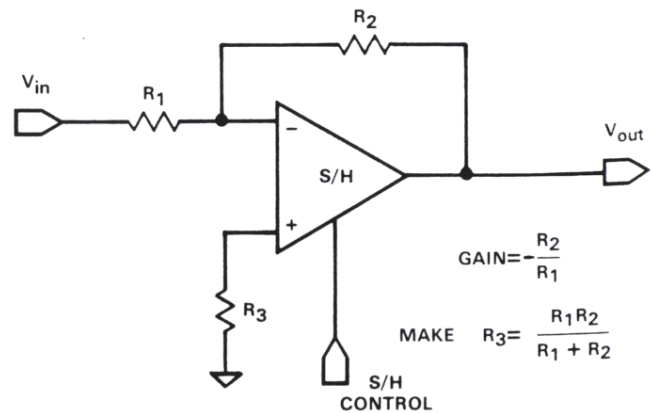


Application No. 3

This illustrates another application in which the hookup versatility of a sample/hold often eliminates the need for a separate operational amplifier and sample-and-hold module. This hookup will have somewhat higher input to output feedthrough during "hold", than the non-inverting connection, since output impedance is the open-loop value during "hold", and feedthrough will be:

$$\frac{V_{IN}R_0}{R_1 + R_2 + R_0}$$

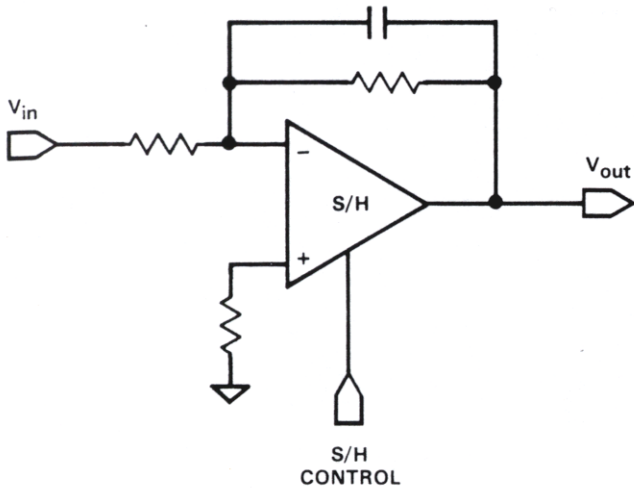
INVERTING SAMPLE-AND-HOLD



Application No. 4

It is often required that a signal be filtered prior to sampling. This can be accomplished with only one device. Any of the inverting and non-inverting filters which can be built with op amps can be implemented. However, it is necessary that the sampling switch be closed for sufficient time for the filter to settle when active filter types are connected around the device.

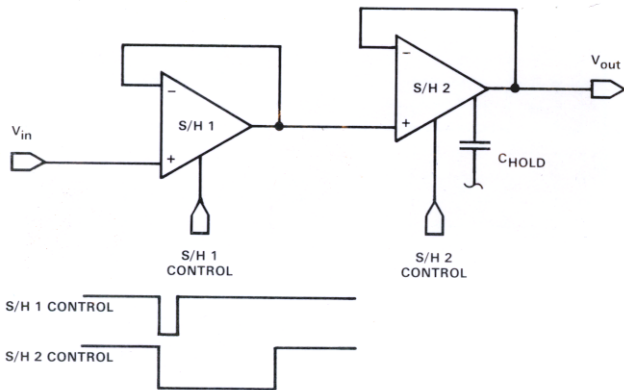
FILTERED SAMPLE-AND-HOLD



Application No. 5

Short sample times require a low value holding capacitor; while long, accurate hold times require a high value holding capacitor. So, achieving a very long hold with a short sample appears to be contradictory. However, it can be accomplished by cascading two S/H circuits, the first with a low value capacitor, the second with a high value. Then the second S/H can sample for as long a time as the first circuit can accurately hold the signal.

CASCADE SAMPLE-AND-HOLD



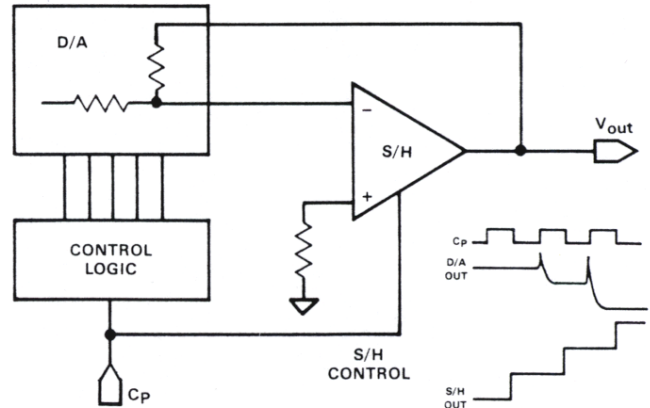
Application No. 6

The word "glitch" has been a universal slang expression among electronics people for an unwanted transient condition. In D to A converters, the word has achieved semi-official status for an output transient which occurs when the digital input address is changed.

In the illustration, the sample/hold amplifier does double duty, serving as a buffer amplifier as well as a glitch remover, delaying the output by 1/2 clock cycle.

The sample/hold may be used to remove many other types of "glitches" in a system. If a delayed sample pulse is required, this can be generated using a dual monostable multivibrator I.C.

DE-GLITCHER

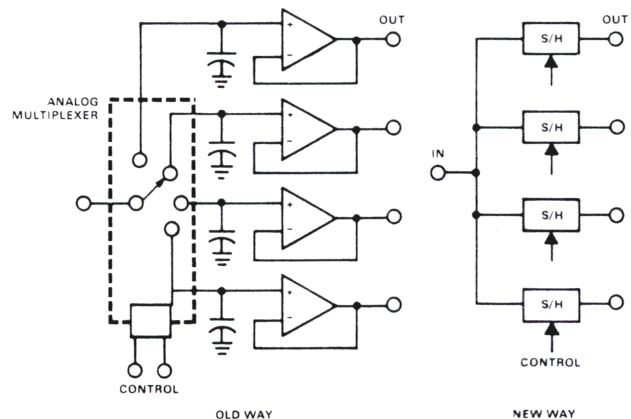


Application No. 7

This circuit reconstructs and separates analog signals which have been time division multiplexed.

The conventional method, shown on the left, has several restrictions, particularly when a short dwell time and a long, accurate hold time is required. The capacitors must charge from a low impedance source through the resistance and current limiting characteristics of the multiplexer. When holding, the high impedance lines are relatively long and subject to noise pickup and leakage. When FET input buffer amplifiers are used for low leakage, severe temperature offset errors are often introduced.

DE-MULTIPLEXER



Application No. 8

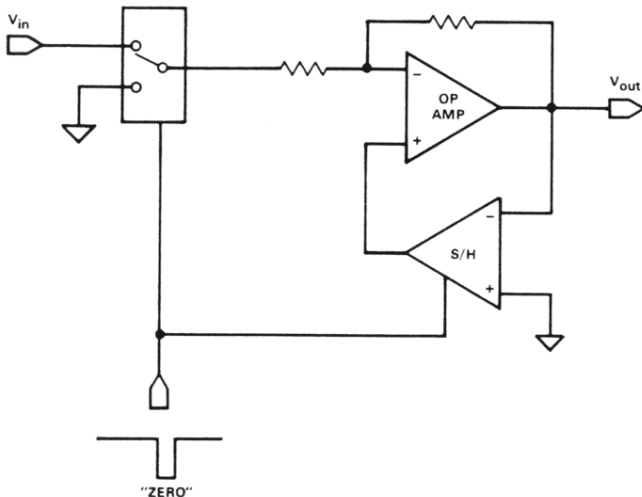
This basic circuit has widespread applications in instrumentation, A/D conversion, DVMS and DPMs to eliminate offset drift errors by periodically rezeroing the system. Basically, the input is periodically grounded, the

output offset is then sampled and fed back to cancel the error.

The system illustrated automatically zeros a high gain amplifier. Care in the actual design is necessary to assure that the zeroing loop is dynamically stable. A second sample-and-hold could be added in series with the output to remove the output discontinuity.

Many variations of this scheme are possible to suit the individual system.

AUTOMATIC OFFSET ZEROING

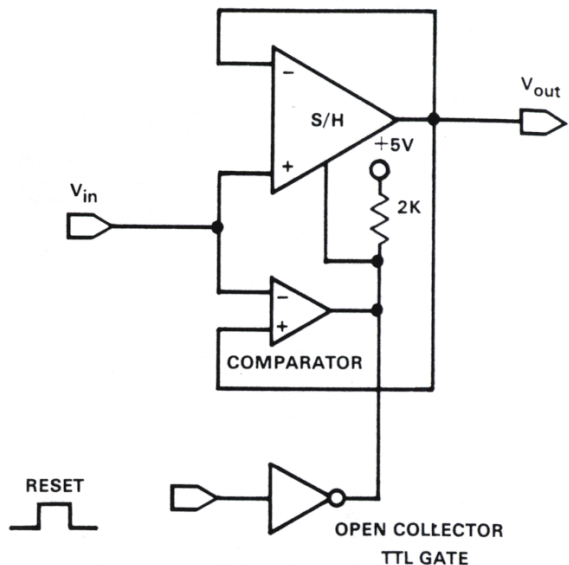


Application No. 9

This accurate, low drift peak detector circuit combines the basic sample-and-hold connection with a comparator. When the input signal level exceeds the voltage being stored in the S/H, the comparator trips, and a new sample of the input is taken. The S/H offset pot should be adjusted for a slight positive offset, so that the comparator will trip back when the new peak is acquired; otherwise the comparator would remain "on" and the S/H would follow the peak back down.

To make a negative peak detector, reverse the comparator inputs and adjust the S/H for a negative offset.

The reset function, which is difficult to achieve in other peak detector circuits, forces a new sample at the instantaneous input level.



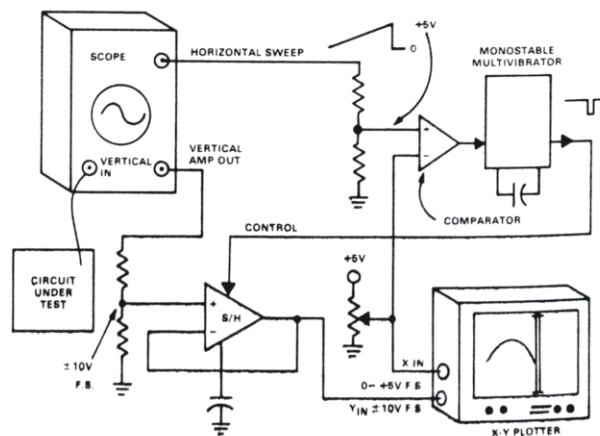
Application No. 10

This useful application illustrates how fast repetitive waveforms can be slowed down using sampling techniques. The input signal is much too fast to be tracked directly by the X-Y recorder, but sampling allows the recorder to be driven as slow as necessary.

To operate, the waveform is first synched in on the scope. Then the potentiometer connected to the recorder X input is slowly advanced, and the waveform will be reproduced. The S/H amplifier samples for a very short interval once each horizontal sweep of the scope. The sampling instant is determined by the potentiometer at the instant when the horizontal sweep waveform corresponds to the X position of the recorder.

This principle can be applied to many systems for waveform analysis, etc.

PLOT HIGH SPEED WAVEFORMS WITH SAMPLING TECHNIQUES



Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.